REMARKS

Claims 1, 2, 4, 6, and 8 are pending in this application. Claim 1 and 4 have been amended to more distinctly claim subject matter which the Applicant regards as the invention.

Claims 1, 2, 4, 6, and 8 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,115,410 to Naruse (hereinafter "Naruse") in view of U.S. Patent No. 6,262,751 to Chan (hereinafter "Chan").

Naruse relates to a Walsh code generator, including a binary counter, a parallel generation controller, and a Walsh code parallel generator. The counter controls the position of an output bit in the Walsh code. The parallel generation controller controls an upper portion of the Walsh code, and the Walsh code parallel generator controls a lower portion of the Walsh code. The parallel generator controller includes a plurality of AND gates, the outputs of the AND gates being connected to a plurality of XOR gates. (See Figures 3-4 and column 5, lines 26-67.)

Chan relates to a display controller for rotating an image to be shown on a computer display, particularly between "landscape" and "portrait" display modes. As shown in Figure 10, the display controller includes three switch stages (94, 96, 98), and each switch stage includes four switch circuits (94a-94d) (column 6, lines 53-57 and column 7, lines 1-15). As noted at column 7, lines 5-8:

> the upper half of the switch circuits in a given stage receives the odd-numbered bits in descending order, while

> the lower ones receive the even-numbered bits in descending order.

In the Office Action on page 2, the Examiner states that Chan "teaches a system wherein the top switch circuit 94a in the first switch bank receives bits 7 and 5, where bit 7 is the most significant bit. Bit 7 is the first bit to be reordered according to Figure 10." Figure 10 of Chan shows the bits being input by grouping odd-numbered bits and even-numbered bits separately in descending order. This is not the same as inputting each binary number in order from most significant bit to least significant bit. In fact, the circuit of Figure 10 can not reorder the bits from least significant bit to most significant bit when they are input in the order of most significant bit to least significant bit. Therefore, the present application is distinguishable over Naruse and Chan because neither reference teaches reordering the bits from least significant bit to most significant bit, when the bits are input in order from most significant to least significant. Pending claims 1, 4, 6, and 8 each disclose inputting the bits in order from most significant bit to least significant bit, and reordering the bits from least significant bit to most significant bit. Neither Naruse nor Chan teach reordering the bits in this manner.

Pending claim 2 contains the reverse step, inputting the bits in order from least significant bit to most significant bit, and reordering the bits from most significant bit to least significant bit. As explained above, neither Naruse nor Chan teach reordering the bits in this manner.

Based on the foregoing amendments and remarks, the combination of Naruse and Chan would not lead one of ordinary skill in the art to the invention recited in pending claims 1, 2, 4, 6, and 8. The Applicant respectfully submits that claims 1, 2, 4, 6 and 8 are in condition for allowance. Accordingly, reconsideration and allowance of the pending claims is respectfully requested.

If the Examiner does not believe that the claims are in condition for allowance, the Examiner is respectfully requested to contact the undersigned at 215-568-6400.

Respectfully submitted,

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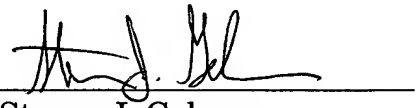
By 
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